On page 1 of the Specification, please insert the following section after the Title and the before the Background Of The Invention:

RELATED APPLICATION

The present application is a continuation of U.S. Application Serial No. 09/687,876 entitled NEAR CHIP SIZE SEMICONDUCTOR PACKAGE filed October 13,2000.

In the Specification:

Please amend the passage of the Specification beginning on page 2, line 27 and ending on page 3, line 9 as follows:

One specific problem with the prior art is that chip sizes differ and/or ~~increases~~ **increase** due to different computing requirements of different products. With existing packaging design, fitting these larger chips means the packages must be made bigger. Bigger packages have larger footprints (the locations where the leads physically and electrically connect to printed circuit boards). The larger footprints forces the printed circuit boards to be redesigned for proper electrical connection. The redesign takes time and money. Thus, a semiconductor package that can fit circuit chips of different sizes without changing the semiconductor package's footprint is needed.

Please amend the passage of the Specification beginning on page 6, line 5 and ending on page 6, line 20 as follows:

DETAILED DESCRIPTION OF THE ~~PREFERRED EMBODIMENT~~ INVENTION

Referring first to FIG. 1, there is shown a perspective cut-away view of a first prior art semiconductor package 50. Semiconductor package 50 is described below to provide a better context for understanding the semiconductor package constructed in accordance with the principles of the present invention. Semiconductor package 50 includes a leadframe 51 (partially shown in Figure 1) having a paddle 52 and a plurality of leads 53. Leads 53 are

located on opposing sides of semiconductor package 50, are generally "Z" shaped, and are spaced parallel and apart from each other. Paddle 52 rests below a horizontal plane defined by the top surface of the top side 57 of leads 53. A semiconductor chip 54 is attached to paddle 52 by using an adhesive. At least a part of semiconductor chip 54 rests below a plane defined by the top side 57 of leads 53. A plurality of bond pads 56 are located on semiconductor chip 54. A plurality of wires 55 electrically connect semiconductor chip 54 (through bond pads ~~54~~ **56)** to leads 53. Bottom side 58 of leads 53 physically and electrically connect the semiconductor package 50 to a printed circuit board (not shown). The above components are affixed in a ~~spacial~~ **spatial** relationship and are protected from the outside environment by sealing material 59.

Please amend the passage of the specification beginning on page 7, line 17 and ending on page 9, line 12 as follows:

Referring to FIGURE 2, there is shown a perspective cut-away view of a second prior art semiconductor package 60. Again, semiconductor package 60 is described below to provide a better context for understanding the semiconductor package constructed in accordance with the principles of the present invention. Semiconductor package 60 has a leadframe 61 (shown partially) having a plurality of leads 62 lined up lengthwise along the two longer sides of semiconductor package 60. ~~Leads~~ **The plurality of leads** 62 are spaced parallel and apart from each other. Each lead in the plurality of leads 62 has an upper part 63 and a lower part 64. A semiconductor chip 65 is placed on top of lower part 64 of leads 62. A plurality of bond pads 67 are located on semiconductor chip 65 for connection to a plurality of wires 66. ~~Wires~~ **The plurality of wires** 66 electrically connect semiconductor chip 65 to **the plurality of** leads 62.

If another semiconductor chip that is larger than semiconductor chip 65 is placed in semiconductor package 60, that larger semiconductor chip will touch and be obstructed by leads 62. Thus, in order to fit a larger semiconductor chip into semiconductor package 60, **the plurality of** leads 62 must be moved outward. Moving **the plurality of** leads 62 outward changes the footprint of semiconductor package 60, thereby forcing a redesign of

the printed circuit board. Again, redesigning the circuit board is undesirable because the redesigning process incurs additional monetary costs and time delays.

Referring now to FIGURE 3, there is shown a perspective cut-away view of semiconductor package 70 that is a first embodiment of a semiconductor package constructed in accordance with the principles of the present invention. Semiconductor package 70 generally ~~consists of~~ **comprises** a leadframe 71 (FIGURE 4), a semiconductor chip 74, a plurality of wires 75, and sealing material 76. A more detailed description of semiconductor package 70 appears below.

Referring now to FIGURE 4, there is shown a detailed perspective view of a leadframe 71 of the first embodiment of a semiconductor package constructed in accordance with the principles of the present invention. Leadframe 71 is made of an electrically conductive material such as, for example, copper. Leadframe 71 has a paddle 72 surrounded by a plurality of leads 73. Leads 73 and paddle 72 are connected to each other via a tie bar ~~71a~~ **78** located on the outer perimeter of leadframe 71. Leads 73 do not touch paddle 72 and are placed parallel and apart from each other. Each one of the leads 73 has a notch 77 at the end near paddle 72. Notch 77 increases the locking strength between leads 73 and sealing material 76 so that leads 73 are less likely to become detached from semiconductor package 70. The bottom of each one of leads 73, after packaging, is exposed to the outside of semiconductor package 70 for electrically and physically connecting semiconductor package 70 to a printed circuit board. To minimize corrosion, the bottom leads 73 are ~~coated~~ **encased** or electroplated with tin, gold, tin lead, nickel palladium, tin bismuth, or other comparable corrosion-minimizing material. Paddle 72 is attached to leadframe 71 through a plurality of ~~connectors~~ **tie bars** 78. Paddle 72 may or may not have a notch (not shown) similar to notch 77 for increasing strength between paddle 72 and sealing material 76. The top side of leads 73 and paddle 72 rest in the same horizontal plane to allow semiconductor chip 74 to be placed on top of both paddle 72 and a portion of leads 73. The bottom of paddle 72 may or may not be exposed to the outer bottom surface of semiconductor **package** 70 **(FIG. 3).**

Please amend the passage of the specification beginning on page 9, line 23 and ending on page 10, line 12 as follows:

Referring still to FIGURE 3, semiconductor package 70 will now continue to be described. A plurality of bond pads 79 are located on semiconductor chip 74 for electrical connection. ~~A~~ **<u>The</u>** plurality of wires 75 electrically connect each ~~bond pad~~ **<u>one</u>** of **<u>the</u>** bond pads 79 to each ~~lead~~ **<u>one</u>** of **<u>the</u>** leads 73. Wires 75 can be made of any electrically conductive material such as, for example, gold, silver, aluminum, or an alloy thereof. Both the lateral side and the bottom side of each one of the leads 73 exposed to the outside of semiconductor package 70 may or may not be coated or electroplated with corrosion-minimizing material such as, for example, tin, gold, tin lead, nickel palladium, tin bismuth, or similar materials. All the components described above are encased (with the exception of the bottom and one lateral side of each ~~lead~~ **<u>one</u>** of **<u>the</u>** leads 73) in sealing material 76. Sealing material 76 may be thermoplastics or thermoset resins, with thermoset resins including silicones, phenolics, and epoxies. Semiconductor package 70 is electrically and physically attached to a printed circuit board (not shown) through any method known in the art of semiconductor package attachment such as, for example, soldering leads 73 to the printed circuit board.

Please amend the passage of the specification beginning on page 10, line 19 and ending on page 12, line 19 as follows:

Referring to FIGURE 6, there is shown a perspective view of leadframe 85 of the second embodiment of a semiconductor package constructed in accordance with the principles of the present invention. Leadframe 85 will now be described in further detail. Leads 81 are connected to each other via a ~~tie bar~~ **<u>frame body</u>** 85a located on the outer perimeter of leadframe 85. Leadframe 85 and leads 81 are made of an electrically conductive material such as, for example, copper. Leads 81 are placed parallel and apart from each other and on opposite sides of leadframe 85. Each ~~one~~ of **<u>the</u>** leads 81 has an inwardly extending member 86 located generally perpendicular to an upwardly extending member 87. The inwardly extending member 86 and the upwardly extending member 87

may be formed ~~thorough~~ **<u>through</u>** a half-etching process. Inwardly extending member 86 extends towards the middle of semiconductor package 80 to support semiconductor chip 82 (shown in FIGURE 5).

Referring back to FIGURE 5, additional components of semiconductor package 80 will now be described. Leads 81 are shown after the trimming process. (The trimming process will be described in more detail later below). Semiconductor chip 82 is attached to leads 81, via an adhesive by using any semiconductor chip attaching processing known in the art of semiconductor packaging. Semiconductor chip 82 can be of different sizes because inwardly extending member of each ~~one~~ of **<u>the</u>** leads 81 has a long upper surface for attaching semiconductor chips of various sizes without having to move the location of leads 81, resulting in a change to the footprint of semiconductor package 80. A plurality of bond pads 88 are located on top of semiconductor chip 82. ~~A~~ **<u>The</u>** plurality of wires 83 electrically connect semiconductor chip 82 (via bond pads 88) to leads 81. The location on leads 81 where wires 83 are bonded to leads 81 may, but does not necessarily have to be, electroplated with gold or silver. Wires 83 are made of an electrically conductive material such as, for example, gold, silver, or aluminum. Sealing material 84 secures leads 81, semiconductor chip 82, and the plurality of wires 83 in a ~~spacial~~ **<u>spatial</u>** relationship. The bottom and one side of each one of the leads 81 rest flush with the outer surfaces of semiconductor package 80 and are exposed to the outside of semiconductor package 80 for electrical and physical connection to a printed circuit board. The electrical and physical connection may, but do not necessarily have to be, achieved through soldering semiconductor package 80 to the printed circuit board (not shown). The exposed surfaces of leads 81 are electroplated with corrosion-minimizing material such as, for example, tin, gold, tin lead, nickel palladium, tin bismuth, or other similar materials known in the art.

Referring now to FIGURE 7, there is shown a perspective cut-away view of semiconductor package 90, which is a third embodiment of a semiconductor package constructed in accordance with the principles of the present invention. Semiconductor package 90 is similar in construction (including the construction of the leadframe) to semiconductor package 80 **<u>of FIGURE 5.</u>**

Semiconductor package 90 differs from semiconductor package 80 in that semiconductor chip 91 is flipped upside down and then attached to the plurality of leads 92 via a plurality of solder balls 93. Solder balls 93 are made of an electrically conductive material and allow a direct physical and electrical connection between semiconductor chip 91 and leads 92. Using solder balls 93 to attach semiconductor chip 91 to leads 92 bypasses the use of wires to electrically connect semiconductor chip 91 to leads 92. The advantage of using solder balls 93 instead of wires to connect semiconductor chip 91 to leads 92 is that using solder balls 93 minimizes the chance of wires breaking or becoming disconnected and causing a failure of the entire semiconductor package 90. In addition, using solder balls ~~83~~ **93** decreases the overall signal induction, thereby ~~exhancing~~ **enhancing** the electrical performance - i.e., speed - of the **semiconductor** package **90.**

Please amend the passage of the specification beginning on page 13, line 11 and ending on page 13, line 24 as follows:

Referring now to FIGURE 9, there is shown a perspective view of a leadframe 105 of semiconductor package 100 prior to the packaging process. Leadframe 105 will now be described first in further detail. Leadframe 105 has a plurality of leads 101 placed generally parallel and apart from each other and along the length of semiconductor package 100. Leads 101 are connected to each other via a ~~tie bar~~ **frame body** 105a located on the outer perimeter of leadframe 105. An equal number of leads 101 may, but does not necessarily have to, rest on each side of semiconductor package 100. Each ~~lead~~ of **the** leads 101 has a notch 106 on the underside of each lead **101**. Notch 106 allows for better locking strength minimizing the chance of ~~a lead~~ **each** of **the** leads 101 from becoming detached from semiconductor package 100. Each one of the leads 101 also has an inwardly extending member 107 extending towards the centerline of semiconductor package 100. The top of all leads 101 rest in one horizontal plane so that semiconductor chip 102 of various sizes can be supported by leads 101.

Please amend the table included on page 15 of the Specification as follows:

~~Attorney Docket No.:~~ **--Application Number--**	**Title of Application**	**First Named Inventor**
~~45475-00015~~ --09/687,485--	Semiconductor Package Having Increased Solder Joint Strength	Kil Chin Lee
~~45475-00016~~ --09/687,487--	Clamp and Heat Block Assembly for Wire Bonding a Semiconductor Package Assembly	Young Suk Chung
~~45475-00019~~ --09/687,495--	Semiconductor Package	Sean Timothy Crowley
~~45475-00020~~ --09/687,531--	Stackable Semiconductor Package and Method for Manufacturing Same	Sean Timothy Crowley
~~45475-00021~~ --09/687,530--	Method and Apparatus for Manufacturing Semiconductor Packages	Jun Young Yang
~~45475-00024~~ --09/687,126--	Method and Apparatus for Manufacturing Semiconductor Packages	Hyung Ju Lee
~~45475-00028~~ --09/687,493--	Semiconductor Package Having Improved Adhesiveness and Ground Bonding	Sung Sik Jang
~~45475-00029~~ --09/687,541--	Semiconductor Package Leadframe Assembly and Method of Manufacture	Young Suk Chung